What is claimed is:

1. A data input and output device comprising:

a timer circuit for counting a value of a count signal, resetting the value of the count signal to an initial value each time the value of the count signal reaches a prescribed value and outputting the value of the count signal at a prescribed interval;

a comparison and coincidence register circuit for storing a setting value, comparing the setting value with the value of the count signal output from the timer circuit and outputting a coincidence signal each time the setting value agrees with the value of the count signal;

a clock selecting circuit for receiving both an external clock signal and each coincidence signal output from the comparison and coincidence register circuit, selecting one of the signals and outputting the selected signal as a data shift clock signal; and

a data shift register circuit for performing a data transmission or reception each time the data shift clock signal is received from the clock selecting circuit.

2. A data input and output device according to claim 1, wherein the comparison and coincidence register circuit comprises

a transmission comparison and coincidence register circuit for storing a setting value corresponding to a data transmission time and outputting a transmission coincidence signal as the coincidence signal each time the setting value agrees with the value of the count signal output from the timer circuit; and

a reception comparison and coincidence register circuit for storing a setting value corresponding to a data reception time and outputting a reception coincidence signal as the coincidence signal each time the setting value agrees with the value of the count signal output from the timer circuit, and

the value of the count signal is cleared to the initial value in the timer circuit each time the transmission coincidence signal output from the transmission comparison and coincidence register circuit or the reception coincidence signal output from the reception comparison and coincidence register circuit is received in the timer circuit.

3. A data input and output device comprising:

a timer circuit for counting a value of a count signal, resetting the value of the count signal to an initial value each time the value of the count signal reaches a prescribed value and outputting the value of the count signal at a prescribed interval;

a comparison and coincidence register circuit for storing a setting value corresponding to a data transmission time and a setting value corresponding to a data reception time, comparing the setting value corresponding to the data transmission time with the value of the count signal output from the timer circuit, comparing the setting value corresponding to the data reception time with the value of the count signal output from the timer circuit, outputting a transmission coincidence signal each time the setting value

corresponding to the data transmission time agrees with the value of the count signal and outputting a reception coincidence signal each time the setting value corresponding to the data reception time agrees with the value of the count signal;

a flip-flop circuit for setting a logical value of a synchronization clock signal to a first value in synchronization with the reception of each transmission coincidence signal from the comparison and coincidence register circuit, setting a logical value of the synchronization clock signal to a second value different from the first value in synchronization with the reception of each reception coincidence signal from the comparison and coincidence register circuit and outputting the synchronization clock signal having two logical values;

a clock selecting circuit for receiving an external clock signal and the synchronization clock signal output from the flip-flop circuit, selecting one of the signals and outputting the selected signal as a data shift clock signal; and

a data shift register circuit for performing a data transmission or reception in synchronization with each logical value of the data shift clock signal received from the clock selecting circuit.

4. A data input and output device according to claim 1, further comprising:

a flip-flop circuit for setting a logical value of a synchronization clock signal of a data transmission and reception in synchronization with the reception of each

coincidence signal from the comparison and coincidence register circuit and outputting the synchronization clock signal.

5. A data input and output device according to claim 1, wherein the value of the count signal is cleared to the initial value in response to each leading edge or each trailing edge of a data signal received by the data shift register circuit.

6. A data input and output device according to claim 3, wherein the value of the count signal is cleared to the initial value in response to each leading edge or each trailing edge of a data signal received by the data shift register circuit.

7. A data input and output device according to claim 1, wherein the setting value of the comparison and coincidence register circuit is stored according to a direct memory access.

8. A data input and output device according to claim 3, wherein the setting value of the comparison and coincidence register circuit is stored according to a direct memory access.

9. A data input and output device according to claim 1, further comprising:

a reload register circuit for sending a new setting value to the comparison and coincidence register circuit each

time the setting value stored in the comparison and coincidence register circuit agrees with the value of the count signal.

10. A data input and output device according to claim 3, further comprising:

a reload register circuit for sending a new setting value to the comparison and coincidence register circuit each time the setting value stored in the comparison and coincidence register circuit agrees with the value of the count signal.

11. A data input and output device according to claim 1, further comprising:

an adder for adding a prescribed value to the setting value stored in the comparison and coincidence register circuit to store a new setting value in the comparison and coincidence register circuit each time the setting value stored in the comparison and coincidence register circuit agrees with the value of the count signal.

12. A data input and output device according to claim 3, further comprising:

an adder for adding a prescribed value to the setting value stored in the comparison and coincidence register circuit to store a new setting value in the comparison and coincidence register circuit each time the setting value stored in the comparison and coincidence register circuit agrees with the value of the count signal.

13. A data input and output device according to claim 1, wherein the value of the count signal counted by the timer circuit is incremented, and the value of the count signal is reset to zero.

14. A data input and output device according to claim 3, wherein the value of the count signal counted by the timer circuit is incremented, and the value of the count signal is reset to zero.